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Substitute for form 1449A/PTO

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(use as many sheets as necessary)

Sheet 1 of 6

Complete if Known

Application Number	10/005,105
Filing Date	December 3, 2001
First Named Inventor	Paul C. Kocher
Art Unit	2132
Examiner Name	Abdulhakim Nobahar
Attorney Docket Number	44424162-8721

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Document Number Number-Kind Code ² (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
/H.N./	V70	US 2,632,058 B1	03-17-1953	Gray	
	V71	US 2,733,432 B1	01-31-1956	Breckman	
	V72	US 3,816,762 B1	06-11-1974	Holt Jr.	
	V73	US 4,268,898 B1	05-19-1981	Brown	
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	V92	US 5,631,492 B1	05-20-1997	Ramus et al.	
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Examiner
Signature

/Abdulhakim Nobahar/

Date
Considered

07/17/2008

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Sheet 2 of 6

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		Number-Kind Code ² (if known)			
/H.N.J.	V95	US 5,859,548 B1	01-12-1999	Kong	
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Examiner Initials*	Cite No. ¹	Foreign Patent Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ³
		Country Code ⁴ Number ⁴ Kind Code ⁵ (if known)				
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/Abdulhakim Nobahar/

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Sheet	3	of	6
OTHER ITEMS - NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	CiteNo. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
/H.N./	V107	DAVIES & PRICE, Security for Computer Networks: An Introduction to Data Security in Teleprocessing and Electronic Funds Transfer, John Wiley & Sons, New York, NY, 2nd Ed., 1989, 377 pages (entire book).	
	V108	Defendant VISA International Service Association's Final Invalidation Contentions for U.S. Patent No. 6,304,658 Pursuant to Patent L.R. 3-6(b), February 8, 2008, Case No. C04-04143 JW(HRL), U.S. District Court, Northern District of California, San Jose Division.	
	V109	Defendant VISA International Service Association's Final Invalidation Contentions for U.S. Patent No. 6,381,699 Pursuant to Patent L.R. 3-6(b), February 8, 2008, Case No. C04-04143 JW(HRL), U.S. District Court, Northern District of California, San Jose Division.	
	V110	Defendant VISA International Service Association's Final Invalidation Contentions for U.S. Patent No. 6,510,518 Pursuant to Patent L.R. 3-6(b), February 8, 2008, Case No. C04-04143 JW(HRL), U.S. District Court, Northern District of California, San Jose Division.	
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	V113	BACK, Adam, "non-interactive forward secrecy", posting to Cypherpunks.Venona.com message board, September 6, 1996. http://cypherpunks.venona.com/date/1996/09/msg00561.html	
	V114	DRAPER, Don et al., "Circuit Techniques in a 266-MHz MMX-Enabled Processor", IEEE J. Solid State-Circuits, pp. 1650-1664, November 1997.	
Examiner Signature	/Abdulahakim Nobahar/		Date Considered 07/17/2008

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			First Named Inventor	Paul C. Kocher	
			Group Art Unit	2132	
			Examiner Name	Abdulahakim Nobahar	
Sheet	4	of	6	Attorney Docket No.	44424162-8721
OTHER ITEMS - NON PATENT LITERATURE DOCUMENTS					
Examiner Initials*	CiteNo. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.			T ²
/H.N./	V115	EBERLE, Hans & THACKER, Charles P., "A 1 GBIT/Second GAAS DES Chip", <u>Proceedings of the 1992 IEEE Custom Integrated Circuits Conference</u> , May 3-6, 1992.			
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	V117	GONZALEZ, Jose Luis & RUBIO, Antonio, "TCMOS: A Low Noise Power Supply Technique for Digital ICs", <u>Electronics Letters</u> , 31(16):1338-1339, August 3, 1995.			
	V118	GREUB, Hans J. et al., "High-Performance Standard Cell Library and Modeling Technique for Differential Advanced Bipolar Current Tree Logic", <u>IEEE Journal of Solid-State Circuits</u> , 26(5):749-762, May 1991.			
	V119	HOUGH, Charles et al., "New Approaches for On-Chip Power Switching Noise Reduction", <u>Proceedings of the IEEE 1995 Custom Integrated Circuits Conference</u> , May 1-4, 1995, pp 133 - 136.			
	V120	IVEY, Peter A. et al., "A Single-Chip Public Key Encryption Subsystem", <u>IEEE J. Solid-State Circuits</u> , 24(4):1071-1075, August 1989.			
	V121	JABLON, David P., "Strong Password-Only Authenticated Key Exchange", <u>Computer Communication Review</u> , ACM SIGCOMM, Univ. of MA., pp. 5-26, September 25, 1996.			
	V122	JARECKI, Stanislaw, "Proactive Secret Sharing and Public Key Cryptosystems", thesis, Massachusetts Institute of Technology, September 1995, Cambridge, MA.			
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Sheet	6	of	6	Attorney Docket No.	44424162-8721
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/H.N./	V132	SCHETTLER, Helmut et al., "A CMOS Mainframe Processor with 0.5- μ m Channel Length", <u>IEEE Journal of Solid-State Circuits</u> , 25(5):1166-1177, October 1990.			
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	V136	TALLINI, Luca G. & BOSE, Bella, "Design of Balanced and Constant Weight Codes for VLSI Systems", <u>IEEE Transactions on Computers</u> , 47(5):556-572, May 1998.			
	V137	TEXAS INSTRUMENTS, SN54LS138, SN54S138, SN74LS138, SN74S138A 3-LINE TO 8-LINE DECODERS/DEMULTIPLEXERS, Texas Instruments, Dallas, Texas, revised March 1988.			
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✓ /H.N./	V139	WILLIAMS, Ted E. & HOROWITZ, Mark, "Bipolar Circuit Elements Providing Self-Completion-Indication", <u>IEEE Journal of Solid-State Circuits</u> , 25(1):309-312, February 1990.			
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